Advanced Wireless CMOS Transceivers

Sunday, February 5, 2006 – San Francisco Marriott

Organizer: **Rudolf Koch**, *Infineon Technologies, Germany*

Committee:
Ken Cioffi, *Discera, San Jose, CA*
Kari Halonen, *Helsinki University of Technology, Finland*
Tony Montalvo, *Analog Devices, Raleigh, NC*
Chris Rudell, *Berkana Wireless, Campbell, CA*
Trudy Stetzler, *Texas Instruments, Stafford, TX*
David Su, *Atheros, Santa Clara, CA*
Francesco Svelto, *University of Pavia, Italy*

Wireless transceiver integration has made dramatic progress in the last decade. GSM phones – single-band, voice-only – started with a component count around 400, employing half a dozen or more chips in different technologies for signal processing alone. Today we see two-chip and even single-chip implementations for wireless LAN or Bluetooth on the market. Cellular phones today routinely cover 3 or 4 bands and support not only voice but also higher data rates. Cameras, MP3 players, outlook support, etc., are added to the basic phone functionality. Whereas two-chip solutions and BiCMOS technologies for the RF frontend are still standard for cellular phones, the first plain CMOS transceivers are available on the market and even single-chip CMOS solutions are sampled.

The next challenges will be the low-cost phone for emerging countries on the one side, and multi-band multi-standard terminals on the other side. Quad-band GSM/EDGE together with UMTS, CDMA for phone functionality, FM radio, digital radio, digital TV for entertainment, Bluetooth and WLAN for connectivity, GPS for localization, navigation and location-based services, and, finally, megapixel camera, iPod functionality , games,… will all be available in a future high-end phone.

Form factor, battery life and production-cost requirements can only be solved by further increasing levels of integration and by re-use and re-configurability of the hardware. How will the mass of components (filters, switches, LNAs, PAs) in the RF frontend be reduced? Will a software-defined radio be superior over hardware-centric implementations for so many standards? Where is the break-even point?

The morning sessions address state-of-the art architectures and design of wireless transceivers. After a short introduction and overview by the organizer, the second speaker, Chris Rudell, will discuss wireless standards and their impact on architectural choices. The next two speakers will look into these architectures in more detail. Tony Montalvo will show the latest aadvances in highly integrated transmitters, e.g. linear I/Q modulators, polar concepts etc. Then, Bill McFarlane, will examine receiver architectures and take a close look at the latest trends, i.e. multiple antennas and on dynamic channel-bandwidth assignment. Finally, Aarno Pärssinen will address the problems arising from the rapidly changing landscape of multi-standad transceivers, and discuss design methodologies supporting quick adaptation to new standards and requirements.

The afternoon sessions will be dedicated primarily to cellular applications. The first two presentations, by Andre Hanke and Bogdan Staszewski, will look into their companies single-chip CMOS GSM transceivers, the first one integrating a proven stand-alone transceiver into a single-chip phone, the second one pursuing digitally-oriented concepts. Finally, Asad Abidi will talk about one of the latest visions in this domain, the software (-defined) radio.

The forum will conclude with a panel discussion, where the attendees have the opportunity to ask questions and to share their views.

Forum Agenda:

Time	Topics
7:00	Served Breakfast for speakers and committee members
8:00	Continental Breakfast for the attendees
Morning session	**Chair: Kari Halonen**
8:30	**Welcome and Introduction** **Rudolf Koch,** *Infineon Technologies, Munich, Germany*
9:00	**Cellular and Short-Range Standards, Key Challenges and their Impact on Architecture** **Chris Rudell,** *Berkana, Campbell, CA*
9:30	**Highly Integrated Linear Transmitters** **Tony Montalvo,** *Analog Devices, Raleigh, NC*
10:15	Break
10:45	**Receivers for Traditional, MIMO, and Dynamic Bandwidth Radio Systems** **Bill McFarland,** *Atheros, Santa Clara, CA*
11:30	**System Design for Multi-Standard Radios** **Aarno Pärssinen,** *Nokia, Helsinki, Finland*
12:15	Lunch
Afternoon Session	**Chair: Franceso Svelto**
1:45	**Transceiver Integration into a Single-Chip Cellular Phone** **Andre Hanke,** *Infineon Technologies, Munich, Germany*
2:30	**Digital RF Processor (DRP) for Cellular Phones** **Bogdan Staszewski,** *Texas Instruments, Dallas, TX*
3:30	Break
4:00	**Software-Defined Radio** **Asad Abidi,** *University of California, Los Angeles, CA*
5:00	Panel Discussion, Q&A
5:30	Conclusion

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Embedded-SRAM Design

Sunday, February 5, 2006 – San Francisco Marriott

Organizer: **Hiroyuki Yamauchi**, *Fukuoka Institute of Technology, Fukuoka, Japan*
Chair: **Don Weiss**, *Intel, Fort Collins, CO*
Committee: **Bruce Bateman**, *T-RAM, San Jose, CA*
Jinyong Chung, *POSTECH, Pohang, Korea*
Kevin Zhang, *Intel, Hillsboro, OR*

Static Random-Access Memory (SRAM) is a dominant memory technology for embedded CMOS-memory applications. Classic 6T SRAM cells can be implemented in most logic-optimized CMOS processes, with few or no additional process steps, and provides a wide range of design flexibilities. Such memory arrays may be optimized for performance (latency and cycle time), functionality (multi-port, multi-bank), and density. Power has become a common limiting factor for embedded applications, from high-performance designs, where power-efficiency is very important, to mobile applications, where battery life is most critical. This forum will cover both ends of the power spectrum, scaling issues with sub-100nm designs, and advances in the test of highly-embedded arrays. Finally, this forum will look out on the horizon for promising new embedded-memory technologies.

Many high-performance VLSI applications, such as microprocessors, demand more and more on-die SRAM memory. Meeting the requirements in both performance and power consumption for such large on-die SRAMs has become increasingly challenging as technology scaling continues. Kevin Zhang will start the forum with some key architecture options/optimizations in large on-die cache-memory designs, and then discuss various circuit-design techniques for achieving high performance. Analysis-and-design tradeoffs for critical circuits will be presented. The design styles for multi-port memory (register files) will also be discussed as it becomes more important in many applications. Some state-of-the-art design techniques for lowering both dynamic and static power consumption, while retaining the high-performance goal, will also be discussed in detail.

At the other end of the power spectrum, mobile applications are driving SRAM-array design to extremely low power and very low voltages. Masanao Yamaoka will describe advanced low-voltage design techniques and the extra-power-reduction design techniques that are required for low active power. The low-leakage design techniques required for low stand-by power will also be presented. Finally, these techniques, as applied to some mobile processors, are presented.

Memories require extensive testing to ensure chip quality, since the vast majority of chip area is occupied by memory. R. Dean Adams will begin by describing how test-pattern selection requires a thorough understanding of the memory design to determine where defects can exist, and how they effect electrical operation. Multi-port designs can introduce even-more possible interactions and opportunities for defects to occur. Redundancy calculation is a significant part of testing to raise memory yield and therefore overall chip manufacturability. All of the needed testing must be accomplished via on-chip logic in the form of a memory built-in self-test (BIST). The BIST applies test patterns to the memory and analyzes the resulting read data. Further design-for-testability (DFT) techniques are utilized to check margins for memory timing and sense-amplifier signal values. All of these DFT factors must be utilized to enable thorough testing of memories.

As device channel lengths shrink down to tens of nanometers, SRAM designs meet new issues and challenges that require changes in the way designs are done. Takayuki Kawahara will reexamine these scaling issues, their impact on cell operation and stability, and design for manufacturability within these new constraints. A new design methodology will be presented. Moreover, soft-error issues, especially those from cosmic rays and those associated with some new kinds of SRAM cells are discussed.

As high-performance multi-core processors are developed along with higher frequencies, SRAM designs must cope with high junction temperatures, fast random-cycle times and high bandwidth, as well as higher-density requirements. In order to meet these requirements, aggressive shrinking, 3D stacking, and other new memory technologies are being developed. Hyun-Geun Byun will address attractive alternatives to conventional 6T SRAM with solutions such as: Pseudo SRAMs, 3D-SRAM, amongst others. In particular, UtRAM, CellularRAM, FCRAM or Cosmo-RAM for mobile applications and BEDDR3 for cache memory, will be discussed.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of embedded SRAM design.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	Introduction
8:40	**High-Performance Power-Aware SRAM Design** **Kevin Zhang**, *Intel, Hillsboro, OR*
9:45	**Low-Power Low-Voltage SRAM Design for Battery Operation** **Masanao Yamaoka**, *Hitachi, Tokyo, Japan*
10:50	Break
11:10	**Design for Testability (DFT)** **R. Dean Adams**, *Magma Design Automation, St. George, VT*
12:15	Lunch
1:00	**Stability/Reliability/Manufacturability Factors in SRAM Design** **Takayuki Kawahara**, *Hitachi, Tokyo, Japan*
2:05	Break
2:15	**Alternatives to 6T SRAM** **Hyun-Geun Byun**, *Samsung, HwaSung-City, Korea*
3:20	Panel Discussion
4:00	Conclusion

Circuit Design in Emerging Technologies

Sunday, February 5, 2006 – San Francisco Marriott

Organizer: **Eugenio Cantatore,** *Philips, Eindhoven, The Netherlands*
Co-Organizer: **Kerry Bernstein,** *IBM, Essex Junction, VT*

Committee: **Anantha Chandrakasan,** *MIT, Cambridge, MA*
Glenn Gulak, *University of Toronto, Toronto, Canada*
Koji Kotani, *Tohoku University, Sendai, Japan*
Siva Narendra, *Tyfone, Portland, OR*
Larry Pileggi, *Carnegie Mellon University, Pittsburgh, PA*
Werner Weber, *Infineon Technologies, Munich, Germany*
C.K. Ken Yang, *University of California, Los Angeles, CA*

The development of the impressive new device technologies we see today is fuelled by a threefold need:

First, CMOS technology requires innovative device architectures and manufacturing approaches to meet the goals of the scaling roadmap.

Secondly, as it becomes more pervasive, electronics needs to evolve alternate forms of mainstream CMOS. These alternatives enable a wealth of emerging applications that traditional CMOS, due to intrinsic limitations, cannot serve. Examples include: large-area and flexible displays, low-cost identification tags, or even spoilage sensors to be embedded in packages.

Finally, limitations to extending the scaling roadmap motivate exploration of innovative ways to improve performance and cost-per-function. Completely new devices and manufacturing technologies potentially achieve much more than simple scaling.

For designers, these developments translate into the challenge to work with new materials, new devices, and innovative fabrication processes. Designers with the ability to combine creativity and novel technologies will lead the development of electronics in the coming era.

This Advanced-Circuit Forum on "Circuit Design in Emerging Technologies" is intended to offer designers an accurate overview of up-to-date design with novel devices, through the words of leading experts in these emerging fields.

The first two presentations address design of CMOS regular fabrics and multigate MOSFETs, of value in the short- and mid-term roadmap. The third and fourth presentations describe both novel (organic-transistor) and mature (Si-TFT) technologies which target applications different than those handled by standard CMOS. The last three presentations describe exciting "end-of-the-roadmap" technologies: Carbon nanotubes and nanowires (for both digital and analog applications) and Spintronics.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of circuit design in emerging technologies.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Welcome and Overview** **Eugenio Cantatore,** *Philips, Eindhoven, The Netherlands*
8:40	**Regular Fabrics for Nano-Scaled CMOS Technologies** **Larry Pileggi,** *Carnegie Mellon University, Pittsburgh, PA*
9:30	**Multigate MOSFET Design** **Gerhard Knoblinger,** *Infineon Technologies, Villach, Austria*
10:20	Break
10:40	**Design with Organic TFTs** **Eugenio Cantatore,** *Philips, Eindhoven, The Netherlands*
11:30	**Technology Trends and Design with Silicon TFTs** **Tatsuya Shimoda,** *Seiko-Epson, Nagano-ken, Japan*
12:20	Lunch
1:20	**Digital Circuits Using Carbon Nanotubes: Modeling, Design, and Architectures** **Ali Keshavarzi,** *Intel, Hillsboro, OR*
2:10	**Analog-Circuit Design with 1D Electronic Devices** **Donhee Ham and Xiaofeng Li,** *Harvard University, Cambridge, MA*
3:00	Break
3:20	**Spintronics: Past, Present, and Future** **Stuart Parkin,** *IBM Almaden Research Center, San Jose, CA*
4:10	Panel discussion
5:00	Conclusion

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Color Imaging

Thursday, February 9, 2006 – San Francisco Marriott

Organizer: **Albert Theuwissen,** *DALSA, Eindhoven, The Netherlands*

Committee:
Dan McGrath, *Eastman Kodak, Rochester, NY*
Jed Hurwitz, *Gigle Semiconductor, Edinburgh, United Kingdom*
Hirofumi Sumi, *Sony, Tokyo, Japan*
Boyd Fowler, *Fairchild Imaging, Milpitas, CA*
Ralph Etienne-Cummings, *John Hopkins University, Baltimore, MD*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Takao Kuroda, *Matsushita, Kyoto, Japan*
Johannes Solhusvik, *Micron Technology, Pasadena, CA*

Color Imaging is a very interesting topic, because the signals that are delivered by the image sensor or the imaging system are not colored at all! Color imaging relies very much on all kinds of signal-processing tricks and optimizations. On the other hand, silicon chips react in a completely different way to color signals than the human visual system reacts. That makes color imaging quite complex and difficult! To contribute to a better understanding of the color imaging, and to stimulate creativity in this field, the ISSCC Subcommittee on Imagers has organized a forum around this theme.

The speakers at the forum are world experts in their fields. They are invited to present up-to-date material on various topics. The presentations are intended to address the material in all of its technical detail.

In the first presentations, the human visual system will be discussed. Certain aspects of color perception are quantitatively summarized in standard color spaces (e.g., CIE-XYZ and CIELAB), and the experimental and biological basis for these color spaces will be explained. The second presentation will provide an overview of color-imaging systems and will discuss which is the best sensor to produce the most-beautiful images.

The third presentation will concentrate on color-filter technology. Important characteristics in filter technology are high integration, overlay, making of the thin film, high sensitivity, and external issues (transport, storage, etc.).

Presentations four and five concentrate on the digital processing of color signals: color matrixing and demosaicing. The quality of the image obtained with a color camera is heavily dependant on the quality of the algorithms used during the matrixing operation and during the demosaicing operation. Both presentations will give an overview of state-of-the-art work in these fields.

It is a property of the human visual system to reduce the effect of illumination when looking at a scene. This property, known as Colour Constancy, is such that a white object is perceived as white independently of the color of the light source. Automatic White-Balance (AWB) algorithms aim to provide an image-capture device with the Same Color Constancy functionality. This is the subject of the sixth presentation.

The last presentation will concentrate on color coding. Digital-camera systems obviously deliver digital-image data, however, there is a wide variety of digital-image standards to which that data can be encoded. In this presentation, the technical parameters of digital-image-exchange standards will be reviewed.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of color imaging.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Welcome and Overview** **Albert Theuwissen,** *DALSA, Eindhoven, The Netherlands*
8:45	**Human Vision System** **Brian Wandell,** *Stanford University, Stanford, CA*
9:35	**Capturing Color Images** **Tetsuya Kuno,** *Mitsubishi, Kyoto, Japan*
10:25	Break
10:40	**Color-Filter Technology** **Katsumi Yamamoto,** *Toppan SMIC Electronics, Shanghai, China*
11:30	**Color Matrixing** **Gennady Agranov,** *Micron, Boise, ID*
12:20	Lunch
1:20	**Color Interpolation** **Takashi Saito,** *Kanagawa University, Yokohama, Japan*
2:10	**White Balancing** **Massimo Mancuso,** *ST Microelectronics, Milan, Italy*
3:00	Break
3:15	**Color Coding** **Charles Poynton,** *ATI Technologies, Toronto, Canada*
4:05	Panel Discussion
4:50	Conclusion

ATAC: High-Speed Interconnect

Thursday, February 9, 2006 – San Francisco Marriott

Organizer/Chair: **Wolfgang Pribyl**, *austriamicrosystems & CONPRI, Graz, Austria*

Committee: **Atila Alvandpour**, *Linköping University, Linköping, Sweden*
Franz Dielacher, *Infineon, Villach, Austria*
Yuriy M. Greshishchev, *PMC-Sierra, Kanata, Canada*
John Long, *Delft University of Technology, Delft, The Netherlands*
Sam Naffziger, *Intel, Fort Collins, CO*
Mehmet Soyuer, *IBM, Yorktown Heights, NY*

This forum will begin with a comprehensive overview of high-speed interconnect techniques, standards, and application areas, given by Yuriy Greshishchev. The next two presentations will discuss requirements and implementation choices for high-speed interfaces in chip-to-chip applications. Christian Sauer and Anthony Sanders will focus on specific challenges in the high-performance processor arena, and in memory systems for consumer applications, respectively.

A variety of techniques for channel equalization, based partly on traditional communications techniques, are available for this field. Evelina Yeung and Bryan Casper will analyze and compare techniques such as linear and non-linear equalization, decision-feedback equalizers, transmit pre-emphasis, continuous-time linear equalizers, etc., with respect to their performance, power, and cost.

The next sequence will deal with 802.3ap 10Gb/s over backplanes (presented by Troy Beukema) and over UTP cables (by Scott Powell). Both presentations will provide an in-depth analysis of architectures, coding schemes, and simulation of those channels, and will compare the results with measured performance data.

As electrical interfaces approach their limits, even with the use of special signal-processing techniques, new techniques, such as optical signaling with integration of photonic and electronic functions on a single silicon (CMOS) chip, are gaining more and more interest. Mario Paniccia will review this field, show recent results, and give a perspective on future developments and opportunities for all-silicon photonics.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of high-speed interconnect.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:30	**Welcome and Introduction** **Wolfgang Pribyl**, *austriamicrosystems & CONPRI, Graz, Austria*
8:40	**High-Speed Interconnect Techniques, Standards and Application Areas** **Yuriy Greshishchev**, *PMC-Sierra, Kanata, Canada*
9:20	**Implementing Chip- and Board-level Protocols on Programmable Platforms** **Christian Sauer**, *Infineon, Munich, Germany*
10:00	**The Evolution of High-Speed Interfaces into Memory Applications** **Antony Sanders**, *Infineon, Munich, Germany*
10:40	Break
11:00	**Receiver Decision-Feedback Equalization for Multi-Gigabit Server Links** **Evelina Yeung**, *Intel, Santa Clara, CA*
11:40	**Tradeoffs of Receive and Transmit Equalization Architectures in 10 to 20 Gb/s I/O Systems** **Bryan Casper**, *Intel, Hillsboro, OR*
12:20	Lunch
1:40	**A Study of FFE/DFE Performance for Application to 10Gb/s 802.3ap Ethernet over Backplane Channels** **Troy Beukema**, *IBM, Yorktown Heights, NY*
2:20	**Multi-Gigabit Signaling Over UTP Cables** **Scott Powell,** *Broadcom, Irvine, CA*
3:00	Break
3:20	**Silicon Photonics in High-Speed Interconnects – Overview, Results, and Future Perspectives** **Mario Paniccia**, Intel, Santa Clara, CA
4:00	Panel Discussion
4:45	Conclusion

Multi-Core Architectures, Designs, and Implementation Challenges

Thursday, February 9, 2006 – San Francisco Marriott

Organizer/Chair: **Peter Kogge,** *University of Notre Dame, Notre Dame, IN*

Committee:
Atila Alvandpour, *Linköping University, Linköping, Sweden*
Georgios Konstadinidis, *Sun Microsystems, Sunnyvale, CA*
Chin-Yi Lee, *National Chiao Tung University, Hsinchu, Taiwan*
Masayuki Mizuno, *NEC, Sagamihara-shi, Japan*
Shannon Morton, *Icera, Bristol, United Kingdom*
Norman Rohrer, *IBM, Essex Junction, VT*
Hector Sanchez, *Freescale, Austin, TX*
Alice Wang, *Texas Instruments, Dallas, TX*
James Warnock, *IBM, Yorktown Heights, NY*

This forum will begin with a presentation by Peter Kogge of the rationale and taxonomy of multicore processing chips (often called Chip-Level Multiprocessors or CMPs) and, what attributes make them attractive, and what are key metrics and design issues.

The next three presentations will describe specific issues in the design of multicore chips, with emphasis on architectural, interconnect, and floor-planning issues, as well as on coping with physical and electrical design constraints. James Laudon will discuss critical issues in designing highly-multi-threaded multicore chips such as Niagara, that are specifically designed for commercial server-level systems. James Kahle will address heterogeneous CMPs that have a particular emphasis on high-end multimedia performance, such as those found in the Cell design. Satoshi Matsushita will address those unique issues associated with mobile embedded multicore technologies, where the given power budget is less than one watt, and real-time response and robustness are important.

The second set of presentations addresses topics related to multicore designs in general, and their effects on overall CAD and design flows. Dan Bouvier will use a high-performance dual-core design to highlight the challenges of interconnecting and integrating a wide range of on- and off-chip interfaces, custom and soft IP. Stefan Rusu will cover circuit-technology aspects of multicore microprocessor design such as clock and power distribution, cache and external bus interfaces, and packaging, thermal and test challenges, with specific examples from Intel CMPs. Finally, Juan Rosal will touch on the many challenges, and current methodologies, related to yield enhancement and test of multicore SoCs for a variety of product arenas, including performance-closure efforts, redundancy schemes, characterization, and modeling that allows for block-level yield enhancement.

This all-day forum encourages open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch will be provided to allow participants to mingle and discuss issues of mutual interest. At the end of the afternoon, all speakers will assemble in a panel format for open discussions with the audience on the challenges in all aspects of Multicore Architectures.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:30	**Welcome** **Peter Kogge**, *University of Notre Dame, Notre Dame, IN*
8:40	**An Introduction to Multicore Chip Design** **Peter Kogge**, *University of Notre Dame, Notre Dame, IN*
9:30	**Niagara: Architecture and Physical Design of a 32-Threaded General-Purpose CPU** **James Laudon**, *Sun Microsystems, Madison, WI*
10:20	Break
10:40	**The Cell Processor's Multicore Architecture: Impact and Influence of Physical Design** **James Kahle**, *IBM, Austin, TX*
11:30	**Low-Power Multicore Chips for Mobile Embedded Applications** **Satoshi Matsushita**, *NEC, Sagamihara, Japan*
12:20	Lunch
1:50	**Challenges of Multicore Processors for Embedded Infrastructure Requiring High-Bandwidth I/O, Memory Interfaces, and On-Chip Accelerators** **Dan Bouvier**, *Freescale Semiconductor, Austin, TX*
2:40	**Circuit Technologies for Multicore Processor Design** **Stefan Rusu**, *Intel, Santa Clara, CA*
3:30	Break
3:50	**Multicore-SoC Test and Yield Enhancement– Challenges and Advancements in a Complex Environment** **Juan Rosal**, *Texas Instruments, Dallas, TX*
4:30	**Panel Discussion: How Does Future Technology Scaling Affect a Multicore World?**
5:00	Conclusion